REMARKS

Claim 1-19 are pending in the application. Claims 2 and 11 have been amended by way of the present amendment. Reconsideration is respectfully requested.

In the outstanding Office Action, claims 2-9 and 11-18 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,469,354 (Hirata) in view of U.S. Patent No. 5,589,423 (White et al.); and claims 10 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata in view of White et al., as applied to claims 2, 7, 11 and 16 above, and further in view of Applicant's Admitted Prior Art (AAPA).

Rejections under 35 U.S.C. Section 103

Claims 2-9 and 11-18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata in view of White et al. Applicants respectfully traverse the rejection.

Claims 2 and 11 have been amended to further clarify the invention. In particular, claims 2 and 11 have been amended to include the phrase "and the I/O pad is located within a p-type semiconductor substrate." Support for the amendment is provided at least by original claim 1 and shown at least in FIG. 1 of the specification. Therefore, the amendments raise no question of new matter.

To establish *prima facie* obviousness of a claimed invention for a §103 rejection, all the claim recitations must be taught or suggested by the prior art. *In re Royka.*[1] All words in a claim must be considered in judging the patentability of that claim against the prior art. *In re Wilson.*[2] (MPEP § 2143.03). When evaluating the scope of a claim, every recitation in the claim must be considered. See e.g. *In re Ochiai.*[3] (MPEP § 2144.08).

Moreover, as noted in § 706.02(j) of the MPEP, three criteria must be met in order to establish a *prima facie* case of obviousness:

(1) the prior art reference (or references when combined) must teach or suggest **all** the claimed limitations;

[1] *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).
[2] *In re Wilson*, 424 F.2d 1382, 165 USPQ 496(CCPA 1970).
[3] *In re Ochiai*, 71 F.3d 1565, 37 USPQ2d 1127 (Fed. Cir. 1995).

(2) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; and

(3) there must be a reasonable expectation of success.

In particular, the teachings or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. Applicants respectfully submit that the prior art does not teach all of the claimed limitations and there is no motivation to modify or to combine the teachings of the prior art.

Hirata discloses a semiconductor device that includes a protective circuit at an input/output port that further includes a plurality of protective MOS transistors.[4] In particular, Hirata discloses input/output circuit sections composed of paired nMOSFETs **31** and pMOSFETs **32**.[5] Further, Hirata discloses the drain regions **14n** of the nMOSFET **31** and the drain regions **14p** of the pMOSFET **32** are connected to another pad **22** via another interconnect **14a**.[6] Further, Hirata discloses the gate electrodes **15n** and **15p** are connected to an output of an un-illustrated output pre-buffer of the internal circuit.[7]

Further, Hirata discloses that the drain **14n** and the source **16n** are formed of an *N+ diffused layer*, and a portion of the P-well **11** located beneath the gate **15n** is of a P-conductivity type, *an NPN parasitic transistor* **12** is formed beneath the gate **15n**.[8] Further, Hirata discloses the drain **14n** corresponds to a collector **14c**, a P-well **11** corresponds to a base **11c**, and the source **16n** corresponds to an emitter **16c** of a parasitic transistor **12.**[9] Furthermore, Hirata discloses the collector **14c** is connected to a pad **22**, and the emitter **16c** is connected to the *ground* together with the guard ring **18n**.[10] Moreover, Hirata discloses a parasitic resistor **17** is formed between the base **11c** and the guard ring **18n**.[11]

However, Hirata nowhere discloses, as amended claims 2 and 11 clearly recite:

> *a silicide blocked p-type field effect transistor* having a source, drain, gate, and gate oxide, said transistor further

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[4] Hirata at ABSTRACT.
[5] *Id.* at FIG. 1A; column 2, lines 4 -5.
[6] *Id.* at FIG. 1A; column 2, lines 5 - 6.
[7] *Id.* at FIG. 1A; column 2, lines 6 - 8.
[8] *Id.* at FIG. 3A;column 2, lines 53 - 56.
[9] *Id.* at FIG. 3A; column 2, lines 57 - 59.
[10] *Id.* at FIG. 3A; column 2, lines 60 - 62.
[11] *Id.* at FIG. 3A; column 2, lines 62 - 63.

> having a snapback voltage that is less than the breakdown voltage of said gate oxide and
>
> wherein said gate is positioned between a p-diffusion of said source and a p-diffusion of said drain,
>
> an n-diffusion is directly connected to said gate and said p-diffusion of said source and the n-diffusion is spaced apart from said p-diffusion of said source,
>
> *said transistor is coupled to an I/O pad that is connected to said p-diffusion of said drain and the I/O pad is located within a p-type semiconductor substrate*, and
>
> the I/O pad has no connection to n-diffusions of said transistor.

That is FIG. 3A of Hirata discloses *an n-type MOSFET* **31** configuration as opposed to "a *silicide blocked p-type field effect transistor,"* as recited in claims 2 and 11 (emphasis added). The outstanding Office Action acknowledges this deficiency in Hirata and attempts to overcome the deficiency by suggesting that "using a silicide blocked p-type field effect transistor is a process limitation which would not carry patentable weight in this claim drawn to structure, because distinct structure is not necessarily produced."[12]

However, it is respectfully submitted that the limitation of "silicide blocked" alone would not make the referenced claims product-by-process claims and thus this limitation should be given patentable weight. At least for this reason, it is respectfully submitted that Hirata does not disclose the claimed invention.

In the alternative, if the referenced claims are still considered by the Examiner as product-by-process claims, it is respectfully submitted that the limitation of "silicide blocked" should still be given patentable weight because a distinct structure is produced in the product. This issue is further discussed below.

With regards to this topic, MPEP § 2113 on Product-by-Process claims states:

> [t]he structure implied by the process steps should be considered when assessing the patentability of product-by-process claims over the prior art, especially where the product can only be defined by the process steps by which the product is made, *or where the manufacturing process steps would be*

[12] Outstanding Office Action at page 3, lines 17-18.

> *expected to impart distinctive structural characteristics to the final product* (emphasis added).[13]

Moreover, MPEP § 2113 further discloses:

> [o]nce the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with *evidence establishing an unobvious difference between the claimed product and the prior art product.*[14]

Applicants respectfully submit that the limitation of "silicide blocked" be given patentable weight because this limitation provides: (1) distinctive structural characteristics of the final product; and (2) an unobvious difference between the claimed product and the prior art product.

In particular, regarding item (1) and item (2), the published application discloses:

> [d]rain resistance **741a** and source resistance **743a** are *facilitated by silicide blocking to increase the level of parasitic resistance* in order to improve current spread across the width of the device (emphasis added).[15]

That is, due to silicide blocking, the distinctive structural characteristics and unobvious differences over the prior art structure of increased levels of parasitic resistance and improved current spread across the width of the device are a part of the claimed invention. Thus, it is respectfully submitted at least for these reasons that "silicide blocked" should be given patentable weight and that Hirata is not obvious over the claimed structure of the invention.

Further, in contrast to FIG. 3A of Hirata, FIG. 7 of the specification clearly shows and claims 2 and 11 recite, "said gate is positioned between a *p-diffusion* of said source and p-diffusion of said drain" (emphasis added). In contrast to the recitations of claims 2 and 11 and the illustration of FIG. 7 of the specification, Hirata clearly discloses, as shown in FIG. 3A, a gate **15n** is positioned between *a N+ diffused area* **16n** of the source and an *N+ diffused area* of the drain **14n**.

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[13] *In re Garnero*, 412 F.2d 276, 279, 162 USPQ 221, 223 (CCPA 1979).

[14] *In re Marosi,* 710 F.2d 798, 802, 218 USPQ 289, 292 (Fed. Cir. 1983).

[15] US Patent Application Publication 2005/0045952 at page 4, paragraph [0040], lines 9-12.

Furthermore, in contrast to FIG. 3A of Hirata, FIG. 7 of the specification clearly shows and claims 2 and 11 recite, "an *n-diffusion* is directly connected to said gate and said *p-diffusion* of said source" (emphasis added). In contrast to the recitations of claims 2 and 11 and the illustration of FIG. 7 of the specification, Hirata clearly discloses, as shown in FIG. 3A, a *P+ type* guard ring **18n** is directly connected to said gate **15n** and an *N+ diffused area* **16n** of said source.

The outstanding Office Action suggests modifying FIG. 3A of Hirata, with the general motivation of being able "to simplify processing steps," to suggest that Hirata can disclose the claimed invention. However, as noted above, Section 2113 of the MPEP states:

> must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings

Therefore, Applicant respectfully requests a citation be provided in Hirata reference that would justify the modification of Hirata to disclose the p-type device of the claimed invention.

Moreover, even if the alternative p-type MOSFET **32** is considered, Hirata nowhere discloses, as recited in amended claims 2 and 11:

> *said transistor is coupled to an I/O pad that is connected to said p-diffusion of said drain and the I/O pad is located within a p-type semiconductor substrate*, and
> the I/O pad has no connection to n-diffusions of said transistor (emphasis added).

That is FIG. 3A of Hirata nowhere discloses "said transistor is coupled to an I/O pad that is connected to said p-diffusion of said drain and the I/O pad is located within a p-type semiconductor substrate," as amended claims 2 and 11 now recite and as shown in FIG. 7 at references **705** and **701**. Thus, the structure of Hirata is *not* identical to the claimed device as suggested in the outstanding Office Action. Therefore, it is respectfully submitted that Hirata nowhere discloses, suggest or makes obvious the invention of claims 2 and 11.

In addition, the outstanding Office Action acknowledges other deficiencies in Hirata and attempts to overcome these deficiencies with White et al.[16] However, White et al. cannot overcome all of the deficiencies of Hirata as discussed below.

White et al. discloses a process for fabricating a non-silicided region in an integrated circuit.[17] However, White et al. nowhere discloses, as amended claims 2 and 11 recite:

> said transistor is coupled to an I/O pad that is connected to said p-diffusion of said drain *and the I/O pad is located within a p-type semiconductor substrate*, and
> the I/O pad has no connection to n-diffusions of said transistor (emphasis added).

That is, White et al. cannot overcome the deficiencies of Hirata, as discussed above. Therefore, Applicant respectfully requests a citation be provided in Hirata reference that would justify the modification of Hirata to disclose the p-type device of the claimed invention.

Therefore, it is respectfully submitted that neither Hirata nor White et al. disclose, suggest or make obvious the claimed invention, whether taken individually or in combination, and therefore, amended claim 2 and claim 11, and claims dependent thereon, patentably distinguish thereover.

Claims 10 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata in view of White et al., as applied to claims 2, 7, 11 and 16 above, and further in view of AAPA. Applicants respectfully traverse the rejection.

Claims 10 and 19 are ultimately dependent upon claims 2 and 11, respectively. Thus, at least for the reasons discussed above, neither Hirata nor White et al. disclose, suggest or make obvious the invention of claims 10 and 19.

In addition, the outstanding Office Action acknowledges deficiencies in Hirata and White et al. and attempts to overcome these deficiencies with AAPA.[18] However, AAPA cannot overcome the deficiencies of Hirata and White et al. as discussed below.

[16] Outstanding Office Action at page 3, lines 17-19.

The AAPA discloses a circuit configuration of the background art typical of a latch-up condition.[19] However, it is respectfully submitted that the circuit configuration of the AAPA is not analogous to the recitations in claims 2, 10, 11 and 19. In particular, amended claims 2 and 11 recite:

> *said transistor is coupled to an I/O pad that is connected to said p-diffusion of said drain and the I/O pad is located within a p-type semiconductor substrate*, and
> the I/O pad has no connection to n-diffusions of said transistor (emphasis added).

That is, the AAPA cannot overcome the deficiencies of Hirata and White et al., as discussed above.

Moreover, claim 10 recites: a "p-type resistor is located between a p-diffusion of said drain of said transistor and said I/O pad" and claim 19 is similarly worded. That is, in the invention of claims 2 and 11, the I/O pad is connected to a *p-diffusion drain* of the transistor. Thus, in claims 10 and 19, the "p-type resistor" is located between the I/O pad and "a p-diffusion drain" of said transistor."

In contrast to the claimed invention, the AAPA discloses a resistor **R** located between an **INPUT PAD** and diodes **D1, D2**. That is, the AAPA nowhere discloses resistor R as connected to a "p-diffusion drain," as clearly recited in claims 10 and 19. Thus, it is respectfully submitted that, the AAPA does not disclose the limitations of claims 10 and 19 and cannot overcome the deficiencies of Hirata and White et al.

Therefore, it is respectfully submitted that none of Hirata, White et al. and AAPA, whether taken individually or in combination, disclose, suggest or make obvious the claimed invention and that claims 10 and 19, and claims dependent thereon, patentably distinguish thereover.

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[17] White et al. at ABSTRACT.

Conclusion

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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[18] Outstanding Office Action at page 5, lines 15-17.
[19] Specification at page 3, lines 20-25.